REMARKS

Status of Claims:

Claims 1-78 are pending in the application. Each of the pending claims defines an invention that is novel and unobvious over the cited art. Favorable consideration of this case is respectfully requested.

Summary of the Present Invention:

The present invention relates to parallel assembly technologies for fabricating multi-layer electronic interconnect structures having vias only between the layers being connected. What differentiates the present invention from the prior art is that the adhesive dielectric which bonds the layers together is inserted between the layers **after** the circuitry and vias have been electrically (and mechanically) connected. Moreover, the present invention relies on the distinction between sequential build-up (SBU) technologies and parallel joining technologies for fabricating multi-layer electronic interconnect structures having vias only between the layers being connected. The present invention is for a parallel joining technology. However, the principal patents cited against the present invention relate to SBU technologies (Lake, et al, US 4,915,983 and Hamilton, GB 2,203,290A). These two reference patents teach nothing related to parallel joining for fabrication of layer to layer connections.

In the earliest multi-layer printed wiring board (PWB) technologies, connections between layers are made by vias drilled through the entire structure after all of the layers have been laminated together. These through via holes are then plated to effect the actual electrical connections between layers, giving birth to the term plated through hole (PTH). The limitation of PTH's for interconnection is that they consume area on all layers of a multi-layer, including those layers above and below the layers being connected. If the PTH were not there, this area on the above and below layers could be used to route more circuitry. For example if I need to connect layers 3 and 4 on a ten layer board, the PTH consumes area on layers 1-2 and 5-10 that is unusable for routing circuitry. Whereas if the via only extended from layer 3 to layer 4, I would be able to route circuitry for other nets on layers 1-2 and 5-10.

To partially alleviate this problem of wasted circuit area, sequential lamination methods were developed. In sequential lamination, two or more multi-layer PWB's are made, each having layers interconnected with PTH's. These are referred to as cores (1-2 layers) or sub-composites (more than 2 layers). The cores and/or sub-composites are then laminated together to form a composite, and connections between layers in different cores and sub-composites are effected with PTH's through the entire composite. What were PTH's in the cores and sub-composites become blind or buried vias in the composite. This sequential lamination method still has significant wasted area because composite PTH's still block area on all layers of the composite, and sub-composite vias block area within a sub-composite.

In order to totally eliminate wasted area due to vias that penetrate layers outside of those connected by the via, a way to make vias that extend only between the layers to be connected is needed. A technology that allows any two adjacent layers to be connected by a via that only penetrates the dielectric between the two adjacent layers can accomplish this. These adjacent layer vias can then be chained together (i.e. a layer 1 to layer 2 via is connected on layer 2 to a layer 2 to layer 3 via to create a layer 1 to layer 3 connection) to connect any 2 arbitrary layers within a multi-layer PWB. Vias within a chain are preferably stacked directly upon one another, as this configuration uses the least area on intermediate layers within a chain, although many technologies have been developed where vias are offset from those immediately above or below, due to difficulties in achieving stacking. There are two known ways to provide this arbitrary via capability, SBU technologies and parallel assembly technologies. For SBU, each additional dielectric plus circuitry layer is fabricated in-situ on top of the previous circuitry layer, each new layer being connected to the previous layer as the new layer is fabricated. The first build-up layer may be fabricated on any base, from an uncircuitized carrier substrate to a multi-layer PWB. For parallel assembly, layers of dielectric with vias and circuitry are fabricated independently of the other layers, and then all layers are joined (connection made between vias and circuitry on independent layers) essentially at the same time.

Parallel assembly technologies would be preferred because they offer lower potential cost than SBU. This is due to the reduced cycle time inherent in parallel vs. sequential process flows,

and higher yield since defective layers can be discarded prior to joining, but with SBU good layers must be discarded with the defective layers to which they are bonded. However, SBU technologies are more widely known and practiced because the processes and materials required are better understood and more generally accessible to those skilled in the arts, and the technical challenges less daunting.

It is the purpose of the present invention to provide a novel and cost effective parallel assembly technology.

Rejections Under 35 U.S.C. § 112, 2nd Paragraph:

Claims 1-45 were rejected under 35 U.S.C. § 112, 2nd Paragraph, as being indefinite.

The Examiner cited claim 1 as being unclear as implying the presence of electrically conductive material on both sides of the dielectric. Claim 1 is hereby amended to recite:

> providing a plurality of sub-composites, wherein each said sub-composite is formed by the steps of
>
> providing a layer of dielectric material having a first surface and a second surface, wherein said first surface is selected from the group consisting of a top surface and a bottom surface,
>
> providing a layer of electrically conducting material on said first surface;
>
> forming at least one blind via comprising a passage from said second surface through said dielectric layer to expose said layer of electrically conducting material.

Claim 1, as amended, clarifies that electrically conductive material is provided only on a first side of a dielectric. Moreover, claim 1 provides that a blind via is formed from a second side of the dielectric and exposes the conductive layer.

Rejection Under 35 U.S.C. § 102(b):

Claims 1-3, 4-10, 12-21, 23-26, 28-33, 36, 42, 45-48, 50-56, and 63-68 were rejected under 35 U.S.C. § 102(b) as being anticipated by Lake (4,915,983).

Rejection under 35 U.S.C. § 102 requires the prior art disclose each and every limitation of the claimed invention (MPEP § 706.02). In determining anticipation, no claim limitation may be ignored. See *Pac-Tex, Inc. v. Amerace Corp.*, 14 USPQ2d 1871 (Fed. Cir. 1990). Anticipation requires the disclosure, in a prior art reference, of each and every recitation as set forth in the claims. See *Titanium Metals Corp. v. Banner*, 227 USPQ 773 (Fed. Cir 1985), *Orthokinetics, Inc. v. Safety Travel Chairs, Inc.*, 1 USPQ2d 1081 (Fed. Cir 1986), and *Akzo N.V. v. U.S. International Trade Commissioner*, 1 USPQ2d 1241 (Fed. Cir 1986). There must be no difference between the claimed invention and reference disclosure for an anticipation rejection under 35 U.S.C. § 102. See *Scripps Clinic and Research Foundation v. Genentech, Inc.*, 18 USPQ2d 1001 (CAFC 1991) and *Studiengesellschaft Kohle GmbH v. Dart Industries*, 220 USPQ 841 (CAFC 1984).

The evidentiary record fails to teach each limitation of the present invention in view of the silence of Lake regarding forming a sub-composite having a conductive layer on only a first side of a dielectric.

At Point 6a. the Examiner states that Lake provides a layer of dielectric material (50) having a top and a bottom. At Point 6b, the Examiner cites Lake as providing a conductive layer (52, 54) on one of the top and bottom of the dielectric. The Examiner refers to Lake, Figure 8. However, Lake at Figure 8 clearly shows a conductive layer (52, 54) on <u>each</u> side of the dielectric. Moreover, at column 8, lines 5-6, Lake recites "[t]he method starts with an insulating material 50 copper foil clad an both sides (step 1, Fig. 8)."

The evidentiary record further fails to teach each limitation of the present invention in view of Lake forming via holes through the conductive layers. The present invention provides conductive material on a first side of an insulator and provides holes from a second side of the insulator to expose the conductive layer. However, Lake provides apertures 56 through the conductive foil. (Column 8, line 8).

Claims 1, 46, and 66-68 were rejected under 35 U.S.C. § 102(b) as being anticipated by Hamilton (GB 2 203 290). The present invention forms blind vias through an insulator to expose

a conductive layer applied thereto. Hamilton forms holes through both the insulator and the conductor. The present invention provides blind vias, whereas Hamilton provides through holes.

Claims 1, 46, and 66-68 were rejected under 35 U.S.C. § 102(b) as being anticipated variously by Shaheen, Katagiri, Rutt, or Hatakeyama. No specific grounds of rejection were advanced.

Rutt relates to dense, substantially parallel, ceramic strata with intervening planar cavities into which conductive material may be introduced. (Column 10, lines 63-69). The present invention provides alternating strata of insulating and conductive materials separated by planar void into which dielectric material may be admitted.

Hatakeyama relates to a method of making a dielectric layer haveing two surfaces covered with conductive foils. The present invention provides the conductive layer on only a first side of the insulator.

Katagiri relates to through holes formed through multiple layers of insulator and conductor (column 8, lines12-15).

Shaheen ('966) etches through holes through a conductor (column 2, lines 15-17).

Shaheen ('855) provides conductor on both sides of an insulator.

Rejection Under 35 U.S.C. § 103(a):

Claims 4, 11, 27, 35, 49, 57-58, and 60-62 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Lake.

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka.* All words in a claim must be considered in judging the patentability of that claim against the prior art. *In re Wilson.* (MPEP § 2143.03). When evaluating the scope of a claim, every limitation in the claim must be considered. See e.g. *In re Ochiai.* (MPEP § 2144.08). The evidentiary record fails to teach each

limitation of the present invention. Specifically, Lake fails to teach the present invention as detailed above.

Claims 22-23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Lake in view of Arndt. Arndt was cited as providing a conductive paste applied with a squeegee. Arndt does not provide the teachings of the present invention, missing from Lake.

Claim Objections:

Claims 1 and 67 were objected to for minor informalities that have been amended per the Examiner's suggestions.

Conclusion:

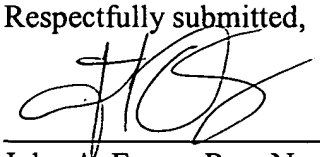
In view of the above, consideration and allowance are, therefore, respectfully solicited.

Accordingly, it is respectfully requested that the foregoing amendments be entered, that the application as so amended receive an examination on the merits, and that the claims as now presented receive an early allowance.

In the event the Examiner believes an interview might serve to advance the prosecution of this application in any way, the undersigned attorney is available at the telephone number noted below.

The Commissioner is hereby authorized to charge any fees or credit any overpayment associated with this communication, including any extension fees or fees for the net addition of claims, to Deposit Account No. 22-0185.

Respectfully submitted,



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APPENDIX: AMENDED CLAIMS
(Claims with markings to show revisions)

1. (Amended) A method for making a multi-layer electronic structure, the method comprising:

providing a plurality of sub-composites, wherein each said sub-composite is formed by the steps of

providing a layer of dielectric material having a first surface and a second surface, wherein said first surface is selected from the group consisting of a top surface and a bottom surface,[;]

providing a layer of electrically conducting material on said first surface [one of the top surface and the bottom surface of the dielectric layer] ;

forming at least one blind via comprising a passage from said second surface through [the] said dielectric layer to expose [the] said layer of electrically conducting material;

depositing electrically conducting material in at least one of [the at least one passage through the dielectric layer] said blind vias wherein said electrically conducting layer is in electrical contact with said electrically conductive material in said at least one blind via;

removing portions of the layer of electrically conducting material to define a pattern of circuitry;

stacking a plurality of said sub-composites [structures comprising the layer of dielectric material and layer of electrically conducting material];

aligning [the] said plurality of sub-composites [structures];

joining [the] said plurality of [structures] sub-composites such that the electrically conducting material in at least one of [the at least one passage through the dielectric material] said blind vias [electrically connects the conductive pattern disposed on the dielectric layer with

another] makes electrical contact with the conductive pattern on [and] an adjacent sub-composite [structure of the stacked plurality of structures]; and

filling spaces between [the structures] adjacent sub composites with electrically insulating material.

67. (Amended) An electronic package, comprising:

a printed wiring board comprising at least two prefabricated substructures joined together, each substructure comprising a layer of dielectric material having a top surface and a bottom surface, a pattern of circuitry on one of the top surface and the bottom surface of the layer of dielectric material, and at least one passage through the dielectric layer in connection with the circuitry, the at least one passage being filled with electrically conducting material, the at least two substructures being stacked on each other such that one of the electrically conducting material filling the at least one passage and the circuitry pattern on one substructure contacts and is electrically conductively joined to one of the electrically conducting material filling the at [lease] least one passage and the circuitry pattern on another substructure; and electrically insulating material between facing substructures except between a joined filled passage and a circuitry pattern; and

a plurality of electronic components attached to the printed wiring board.